EBI Registers Configuration Application Note V1.0

Publication Release Date: Sep. 2008

Support Chips:

NUC710A

NUC745A

Support Platforms:

All

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1. Introduction

The External Bus Interface (EBI) controls the access to external memory (NOR Flash, SDRAM) and external I/O devices. This document describes how to configure EBI registers of different devices. Hardware connection is beyond the scope of this document.

2. Register Configuration

2.1. EBICON

EXBE0~EXBE3 only need to be set to 1 while the external I/O bank is connected with a SRAM device. Otherwise, leave them as 0. One of *REFEN* and *REFMOD* should be set at 1, and the other should be cleared to 0. During normal operation, *REFEN* should be 1, and *REFMOD* should be 1 if CPU wishes to enter power down mode. *CLKEN* should set to 1 during normal operation and cleared to 0 during power down mode. *REFRAT* configures the refresh cycle of SDRAM controller. It is calculate with period = value /fMCLK. *WAITVT* only take effect if external device comes with nWAIT signal and connect with CPU's nWAIT pin, and GPIO30 is configured as nWAIT function. Its value should be set according to external device.

2.2. ROMCON

BASADDR is used to set the base address of ROM/flash bank. From system memory map, whole memory space is divided into 2GB cacheable memory space and 2GB non-cacheable memory space. Which also indicates address bit 31 is used to control bus access behavior. So what needs to be fill into this field is the bit 30~18 of the base address. For example, to set the ROM/flash base address at 0x7F000000 (non-cacheable address is at 0xFF000000), simply left shift the address for one bit, and fill bit 31~19 into BASADDR, which is 1111111000000b. *SIZE* should be consistent with the actual ROM/flash size. *tPA* and *tACC* should match the timing diagram shown in RAM/flash's datasheet. *BTSIZE* is decided from power on setting, software does not need to modify this field. For most ROM/flashed, the last field, *PGMODE*, could be kept at 0. Please refer to ROM/flash's datasheet to check if this field needs to be configured with other value.

2.3. SDCONFx

The method of calculating *BASADDR* is the same with **ROMCON**. Please refer to section 2.2 for the setting of *BASADDR*. Write 1 to *MRSET* will issue a mode register set command to SDRAM. This bit clears itself to 0 afterward. It is strongly recommend user to set this bit whenever the value of **SDCONFx** needs to be changed. *AUTOPR* must always keep at 0. Proper *LATENCY* setting could be found in SDRAM datasheet. *COMPBK* could also be found in SDRAM datasheet. *DBWD* should be consistent with the hardware connection. Proper *COLUMN* setting could be found by look up the AHB Bus Address Mapping to SDRAM Bus table in section 6.3.2.1. Please note, users should use the type of single SDRAM chip to search the table. *SIZE* sets the SDRAM size on each bank.

Here're two examples to demonstrate how to configure these registers.

Example1. Two Winbond 986416EH-6 SDRAM connects on BANK0, and nothing on BANK1. (This example is valid on NUCP710A only since NUC745A does not support 32 bit bus width)

Since nothing is connecting on BANK1, simply leave it with the reset value. The SDRAM should locate at address 0, so *BASADDR* is 0. From the general description in datasheet, user can know this is a CL3 SDRAM, which means CAS latency should be 3. Hence *LATENCY* should be set to 10b.

From the datasheet header, user can know this SDRAM has four banks, so *COMPBK* should set 1.

1M × 4 BANKS × 16 BITS SDRAM

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Each SDRAM provides 16 bit data width, 2 SDRAM provides 32 bit data bus totally. So *DBWD* should be 11b.

The SDRAM 1M x 4 Banks x 16 bits, and total bus width is 32 bit, so users should look into SDRAM Data Bus Width – 32 bits table, search for 4M x 16 SDRAM, and from R x C column, users can find the column number is 8. So *COLUMN* should be 00b.

SDRAM Data Bus Width: 32-bit

Total	Type	R x C	R/C	A14 (BS1)	A (B
16M	2Mx8	11x9	R	**	
			C	**	
16M	1Mx16	11x8	R	**	
			C	**	
64M	8Mx8	12x9	R	11	
			C	11	
64M	4Mx16	12x8	R	11	

The total size of SDRAM is 16 MB, so *SIZE* should be 100b. Combined the information above, SDCONF0 should be filled with 0x90E4.

Example2. Both BANK0 and BANK1 connect with one Winbond 986416EH-6 SDRAM.
Follow the previous example. User can know the proper value of *LATENCY* and *COMPBK*.

The *BASADDR* of BANK0 is of course 0, the size of SDRAM is 8MB. So the base address of BANK1 should set to 0x800000. Left shift this value for one bit. User can get the value of *BASADDR*, which should be 0000000100000b.

Data bus of both BANK0 and BANK1 is now 16 bits, so *DBWD* should be 10b. And size of each bank is 8MB, so *SIZE* should be 011b.

Look into SDRAM Data Bus Width -16bit table and search for 4M x16 type SDRAM, user can get the column address as 8 bits. So *COLUNM* should be 00b.

SDRAM Data Bus Width: 16-bit

Total	Type	R x C	R/C	A14 (BS1)	A13 (BS0)	A12
16M	2Mx8	11x9	R	**	10	**
			C	**	10	**
16M	1Mx16	11x8	R	**	9	**
			C	**	9	**
64M	8Mx8	12x9	R	10	11	10
			C	10	11	10
64M	4Mx16	12x8	R	10	9	10

Combined pervious information, the value of SDCONF0 and SDCONF1 should be configured as 0x90C3 and 0x10090C3 respectively.

2.4. SDTIMEx

tRCD, *tRDL*, *tRP*, and *tRAS* configures the timing characteristic of SDRAM control signals. Please refer to the datasheet of on board SDRAM to set the proper value of these fields.

2.5. EXTxCON

These registers control the interface towards external I/O devices. The method of calculating *BASADDR* is the same with **ROMCON**. Please refer to section 2.2 for the setting of *BASADDR*. *SIZE* is used to configure address space size reserve for this bank. *ADRS* is usually set with 0. While it is 0, AHB bus's A1 will send to A0 of external device, A2 will send to A1 of external device… while data bus width is 16 bits. And AHB bus's A2 will send to A0 of external device, A3 will send to A1 of external device… while data bus width is 32 bits. This is usually how the external device should work. However with some external devices, no matter the data bus width is 8, 16, or 32 bits, its A0 is expecting the value from AHB A0, A1 is expecting A1 from AHB A1… in such case, *ADRS* should set to 1. *tACC*, *tCOH*, *tACS*, and *tCOS* configures the characteristic of external I/O bank timing. Please refer to the figures of External I/O read/write operation timing and the data sheet of external device to set the proper values into these fields. *DBWD* configures the data bus width of external bank. This value must be consistent with the hardware connection.

2.6. CKSKEW

This register adjusts the clock skew of SDRAM. The value set by bootloader, 0x0FF0039, is usually fairly safe. However, if this value does not fit users' hardware, Nuvoton can provide an application to measure proper value.

3. Revision History

Version	Date	Description
V1.0	Sept. 2008	● Created

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